

# **User Manual for PCIe to UART Controller**

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## 1 Introduction

### 1.1 Purpose

The purpose of this document is to explain the procedure to power-on and setting up working environment of the PCIe to UART controller for demo purpose.

### 1.2 Scope

This document describes the Hardware connection procedure to power-on and establishes Serial communication with PC.

### 1.3 Features

#### PCIe Interface

- The Xilinx endpoint cores for PCIe follows PCI express base specification v1.1 layering model
- 32-bit internal data path
- The endpoint core implements the physical layer, datalink layer, transaction layer & configuration management layer
- Six individually programmable BAR's & expansion ROM BAR
- Supports MSI & INTX emulation
- Supports removal of corrupt packets for error detection and recovery
- Compatible with PCI/PCI Express power management functions
- Used in conjunction with NXP PX1011A PCI Express standalone PHY to achieve high transceiver capability, 2.5 GBPS line speed, automatic clock and data recovery, 8b/10b encode and decode
- Supports a maximum transaction payload of up to 512 bytes

#### UART Controller Interface

- The UART bridge uses IO mapped interface
- Full duplex asynchronous communication
- Baud rate of 115200 with a single odd parity, stop & start bit
- Supports transmit & receive FIFO of size 16 byte depth

### 1.4 Evaluation Board and Core requirements

- Spartan-3 PCI Express Kit
- Mother Board with PCIe slot with PCIe tree software installed
- PC/laptop with an available COM port
- 9-pin RS-232 Serial cable
- Endpoint core for PCI express from xilinx
- PCIe to UART controller core

## 2 PCIe to UART Controller Core

### 2.1 Block Diagram

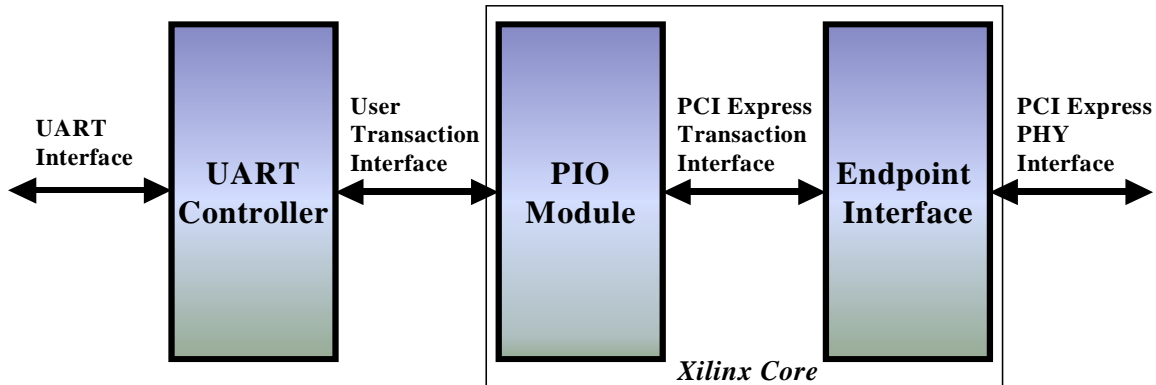


Figure 1: Detailed view of iW-PCIe to UART Controller core

### 2.2 Description

The PCIe Bridge has an endpoint PIPE v1.7 (PHY Interface) for PCIe 1 lane core from Xilinx, Programmed I/O module & UART controller. The endpoint core from xilinx implements the physical layer (PHY interface), data link layer, transaction layer & configuration management layer of PCIe base specification v1.1 layering model. The PIO design interfaces with the endpoint for PCI Express core's transaction interface & responds with read/write transaction for memory or IO transaction from the endpoint core.

The UART controller is implemented in user interface side of the PIO design. The serial controller Unit supports for asynchronous communication only. The processor can access the unit through I/O read and write commands. The SCU converts parallel data from the host processor to serial data and transmits it and converts the serial received data into parallel data for the host processor to read. The start bit, parity bit and the stop bits are automatically added in the transmit direction and is stripped in the receive direction.

### 2.3 Pin outs of PCIe to UART Controller core

The pin outs of iW- PCIe UART Bridge is as shown in the table below.

**Table 1: Pin outs of iW-PCIe UART Bridge**

<b>iW-PCIe UART Bridge PINS</b>	<b>FPGA PINS</b>
powerdown[0]	AF22
powerdown[1]	AD23
resetsn	AF24
rxpolarity	AE24
txclk	AE21
txcompliance	AE23
txdata[0]	AD15
txdata[1]	AE15
txdata[2]	AF15
txdata[3]	AE19
txdata[4]	AF19
txdata[5]	AE20
txdata[6]	AF20
txdata[7]	AD21
txdatak[0]	AE22
txdetectrx_loopback	AF21
txelecidle	AF23
phystatus	AF12
rxdata[0]	AE8
rxdata[1]	AC7
rxdata[2]	AF6

<b>iW-PCIe UART Bridge PINS</b>	<b>FPGA PINS</b>
rxdata[3]	AE6
rxdata[4]	AD6
rxdata[5]	AC6
rxdata[6]	AE5
rxdata[7]	AD5
rxdata[0]	AF8
rxlecidle	AF4
rxstatus[1]	AD10
rxstatus[2]	AC11
rxvalid	AD12
rxclk	AE13
sys_reset_n	AE4
txd_o	AB11
rx_d_i	AA11
baud_clk_i	B14



## 3 Quick Start

### 3.1 Connecting to a Host computer

Follow the steps below to connect the Spartan-3 PCI Express to the host computer to test the functionality of iW-PCIe Bridge core.

#### 3.1.1 Installation Requirements

The items listed below are necessary to install Spartan-3 PCI Express to the host computer

- PC/laptop with an available COM port.
- Host computer of windows NT/2000 or windows XP OS having an available PCIe slot, with installed PCIe Tree software.
- RS232 serial cable.

#### 3.1.2 Board Installation & Testing

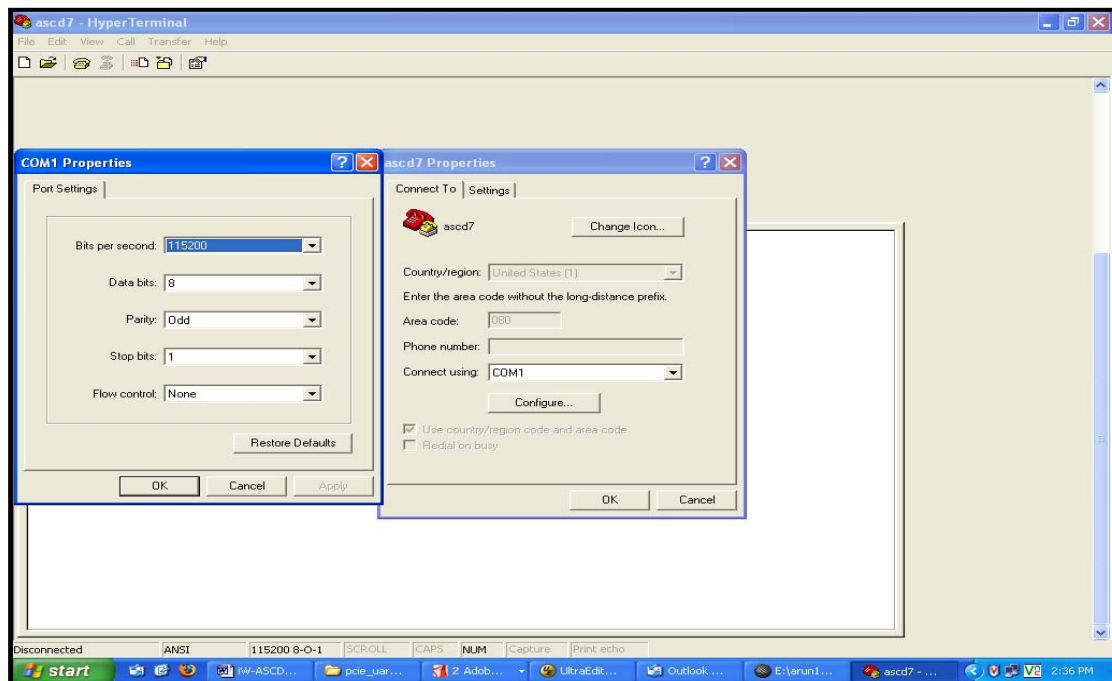
1. Before connecting Spartan-3 PCI Express Kit in the PCIe slot check all these settings are properly done for starter kit
  - Select the master parallel mode for FPGA configuration by installing M2 in JP3 Header.
  - Other Jumpers position on Board, JP8 2-3, JP1 2-3, JP2 2-3, JP5 1-2, JP6 2-3, JP9, J4.
  - Select the power source from the PCIe edge connector for this install the fuse in socket F2 position (dont place separate fuse in F1 position).
  - Install the clock source of 24.576 Mhz in the user clock socket U10 for baud clock generation.

After this settings place the board in PCIe slot of a host computer.

2. Connect the RS232 serial cable one end to the DB9 connector P1 on Spartan-3 PCI Express board and the other end to the DB9 connector of a PC/laptop which hyper terminal installed, set the hyper terminal properties as in the hyper terminal screen shot.
3. Program the MCS file pcie\_uart\_bridge.mcs provided with user manual to the Spartan-3 PCI Express board by connecting Xilinx platform USB cable from PC USB port to , for this first program the on-board 8 Mb xilinx XCF08P parallel Platform Flash PROM then configure the FPGA from the image stored in the Platform flash PROM by power cycling (switch off & on the board).
4. Run the PCItree software on the host computer where the Spartan-3 PCI Express board is installed.
5. Check the software overview part to get more information regarding Pcitree software for read & write of memory & io space of host computer.

### 3.2 Procedure for demo

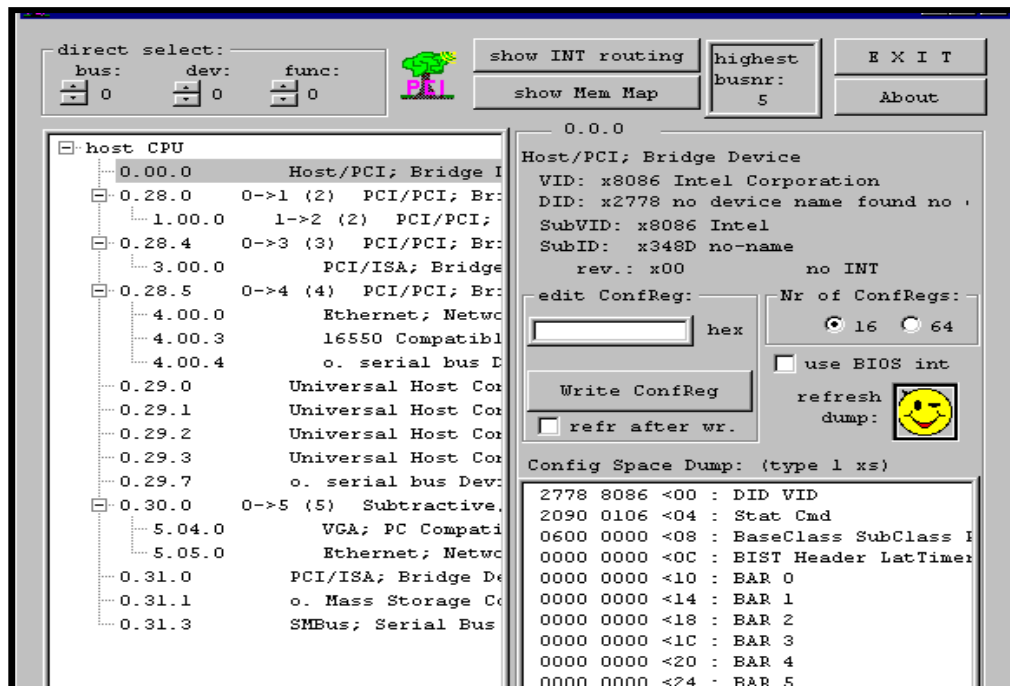
- Connect Spartan-3 PCI Express board to the PCIe slot of host computer also connect the RS232 serial cable to the board & the serial port of a computer/laptop.
- Open the HyperTerminal on PC/Laptop with following settings
  - Baud rate: 115200 bps
  - Data bits: 8
  - Parity: odd
  - Stop bits: 1
  - Flow control: none, then press OK



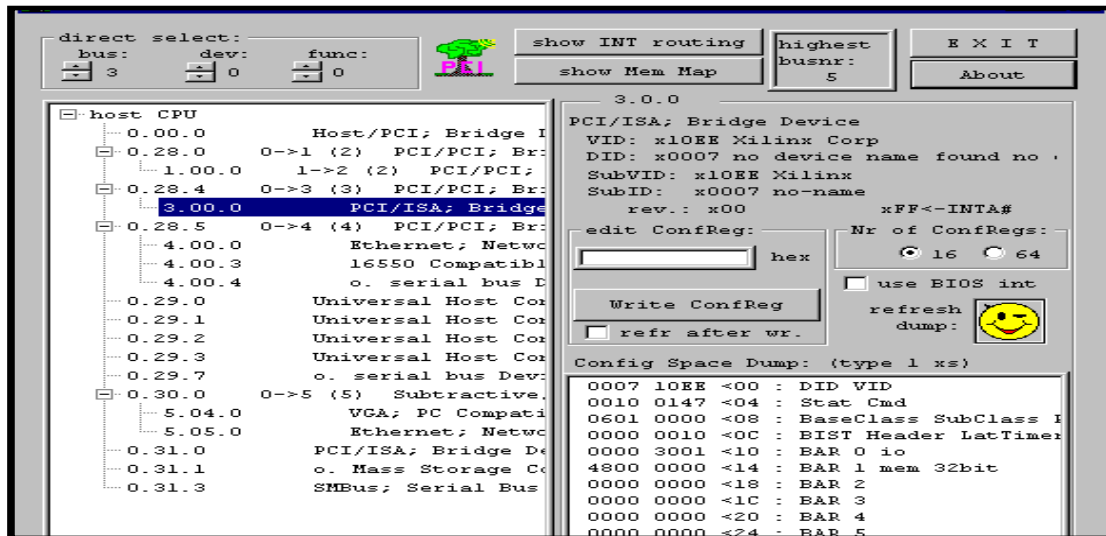
- Start the PCItree software installed in the host computer to which Spartan-3 PCI Express board is connected, then Press OK



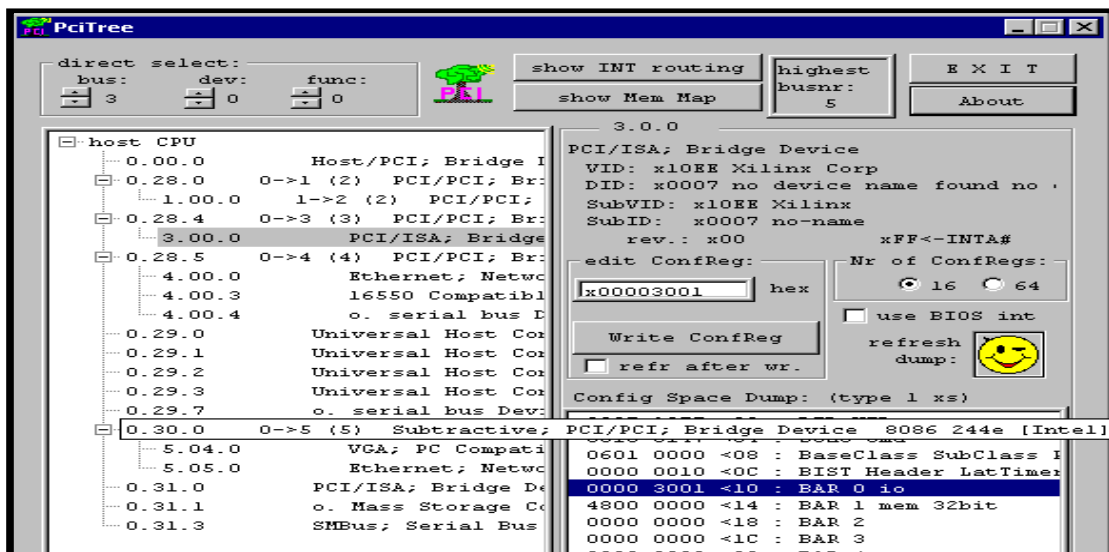
- The software will scan all the PCI bus attached to the host computer & displays all the PCI bus as the tree structure. Each PCI component has an integer number for bus, device and function (bdf).



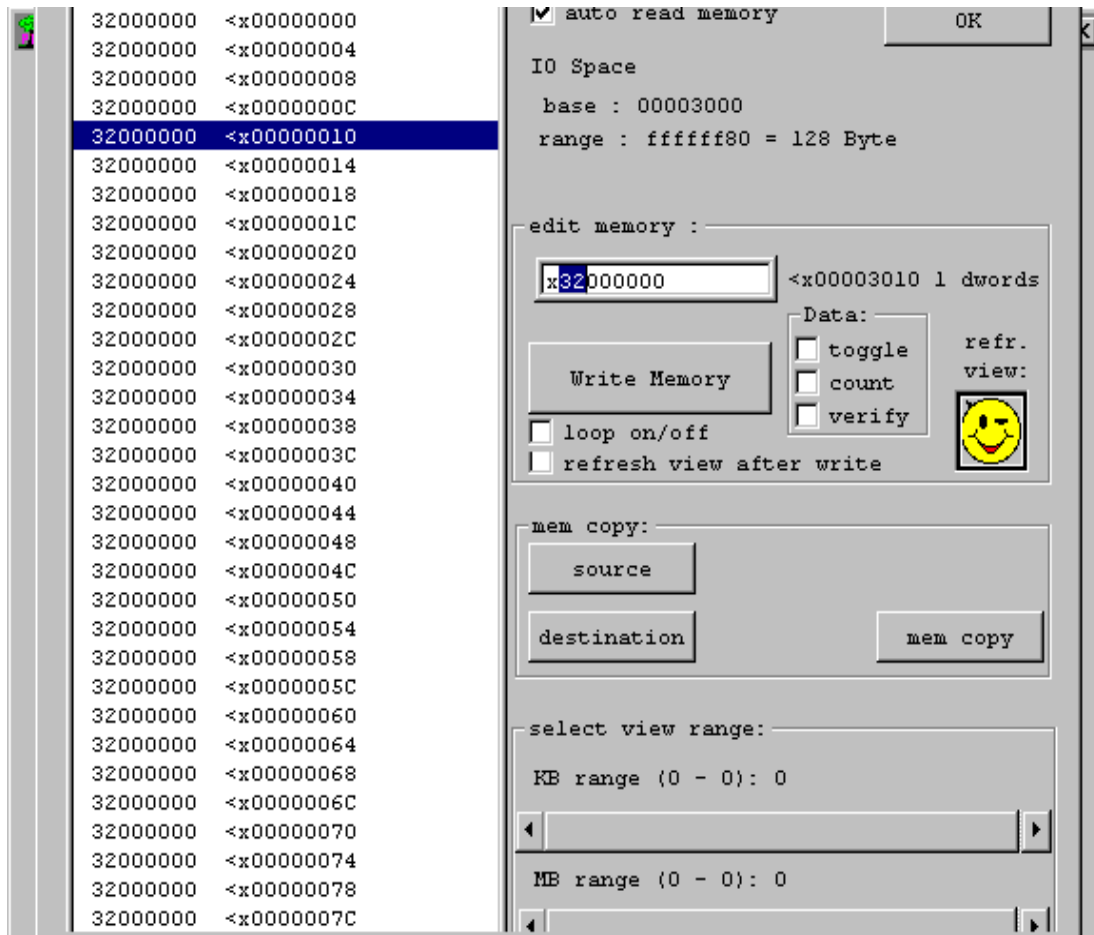
- Locate the Spartan-3 PCI Express board in the PCI bus list once you locate the device PCITree software will displays bus number, device number, function number, Vendor ID, device ID & configuration space contents in the right side of the pcitree window.



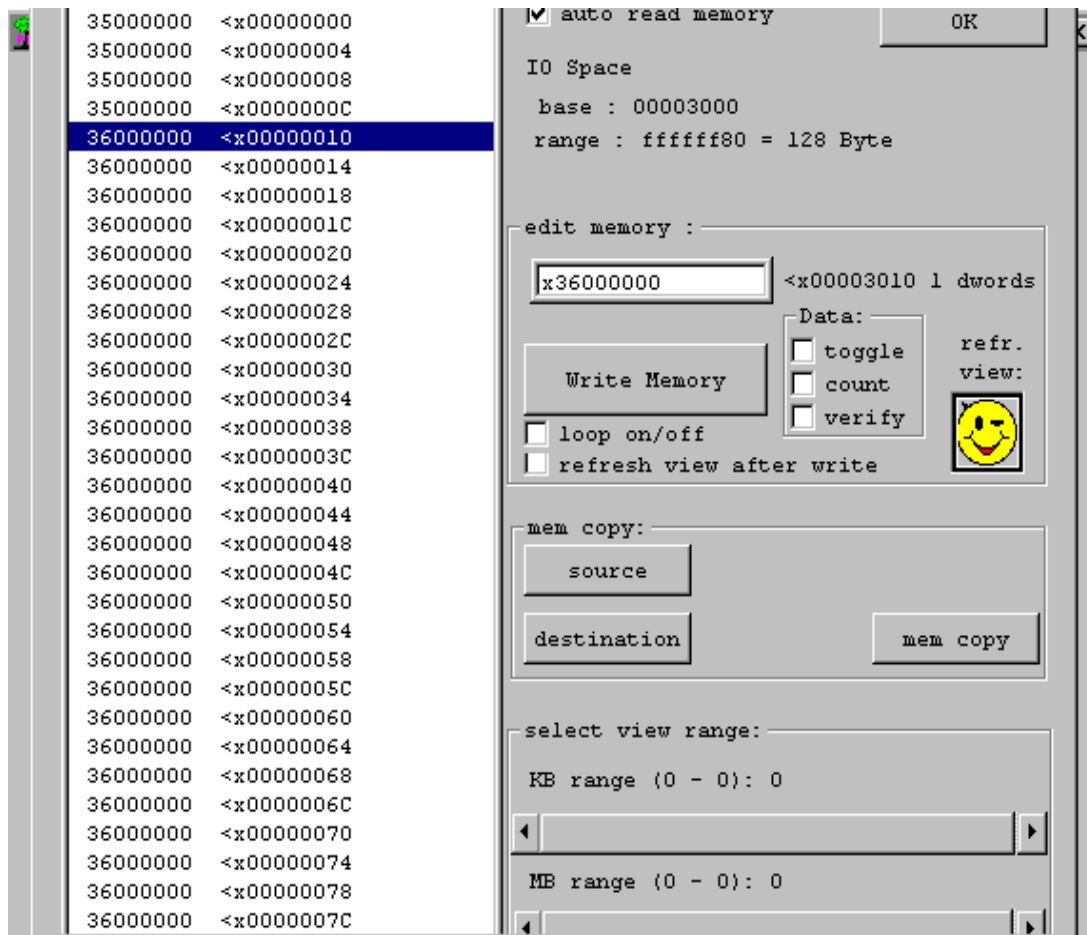
- Select the BAR register, now UART bridge is mapped to BAR 0 (IO bar at address location 00000010h) locate the BAR 0 register to test the UART bridge functionality. Double click on the BAR 0 register position to access the IO register mapped to BAR 0.



- Open the hyper terminal on the PC/laptop, locate the IO address location 00000010h to write & read the buffer registers of UART in the PCItree window, in the edit memory tab enter some ascii value of data then press enter, the data as to come in the hyper terminal. We can observe digit 2 on the hyper terminal.



- To check the receiver path enter some data on the hyper terminal window & try to read it back from the host cpu by selecting auto read memory also locate the IO address location 00000010h & then press refr view tab to read the received data. We can observe the data entered in the hyper terminal to reflect on the 00000010h register contents



## APPENDIX A

### Reference Documents

- ❖ PCItree software usage from - <http://www.pcitree.de/userguide.html>
- ❖ Spartan-3 for PCI Express starter kit board user guide UG256 - [http://www.xilinx.com/support/documentation/boards\\_and\\_kits/ug256.pdf](http://www.xilinx.com/support/documentation/boards_and_kits/ug256.pdf)